奇美電子 CHIMEI INNOLUX

PRODUCT SPECIFICATION

□Tentative Specification
□ Preliminary Specification
■ Approval Specification

MODEL NO.: V315B5
SUFFIX:L13

Customer：

APPROVED BY **SIGNATURE**

Name / Title _____ _____

Note

Please return 1 copy for your confirmation with your signature and comments.

Approved By	Checked By	Prepared By
Chao-Chun Chung	Josh Chi	Chloe Chen

CONTENTS -

REVISION HISTORY ---------- 3

1. GENERAL DESCRIPTION ---------- 4
   1.1 OVERVIEW
   1.2 FEATURES
   1.3 APPLICATION
   1.4 GENERAL SPECIFICATIONS
   1.5 MECHANICAL SPECIFICATIONS

2. ABSOLUTE MAXIMUM RATINGS ---------- 5
   2.1 ABSOLUTE RATINGS OF ENVIRONMENT
   2.2PACKAGE STORAGE
   2.3ELECTRICAL ABSOLUTE RATINGS

3. ELECTRICAL CHARACTERISTICS ---------- 7
   3.1 TFT LCD MODULE
   3.2 CCFL(Cold Cathode Fluorescent Lamp) CHARACTERISTICS

4. BLOCK DIAGRAM ---------- 13
   4.1 TFT LCD MODULE

5. INTERFACE PIN CONNECTION ---------- 14
   5.1 TFT LCD MODULE
   5.2 BACKLIGHT UNIT
   5.3 INVERTER UNIT
   5.4 LVDS INTERFACE
   5.5 COLOR DATA INPUT ASSIGNMENT

6. INTERFACE TIMING ---------- 20
   6.1 INPUT SIGNAL TIMING SPECIFICATIONS
   6.2 POWER ON/OFF SEQUENCE

7. OPTICAL CHARACTERISTICS ---------- 24
   7.1 TEST CONDITIONS
   7.2 OPTICAL SPECIFICATIONS

8. DEFINITION OF LABELS ---------- 28
   8.1 CMO MODULE LABEL

9. PACKAGING ---------- 30
   9.1 PACKING SPECIFICATIONS
   9.2 PACKING METHOD

10. PRECAUTIONS ---------- 32
   10.1 ASSEMBLY AND HANDLING PRECAUTIONS
   10.2 SAFETY PRECAUTIONS

11. MECHANICAL CHARACTERISTICS ---------- 33

REVISION HISTORY

Version	Date	Page (New)	Section	Description
Ver 2.0	Jan 19, 11'	All	All	Approval Specification was first issued.

1. GENERAL DESCRIPTION

1.1 OVERVIEW

V315B5- L13 s a 31.5" TFT Liquid Crystal Display module with 4U-type CCFL Backlight unit and 1ch-LVDS interface. This module supports 1366 x 768 WXGA format and can display 16.7M (8-bit/color)colors. The inverter module for backlight is built-in.

1.2 FEATURES

-High brightness (450 nits)
- Ultra-high contrast ratio (3500:1)
- Fast response time (gray to gray average 8.5ms)
- High color saturation NTSC 72%
- Ultra wide viewing angle : 176(H)/176(V)(CR≥20)with Super MVA technology
- DE (Data Enable) only mode
- LVDS (Low Voltage Differential Signaling) interface
- Color reproduction (nature color)
- Low color shift function

1.3 APPLICATION

- TFT LCD TVs
- Multi-Media Display

1.4 GENERAL SPECIFICATI0NS

Item	Specification	Unit	Note
Active Area	697.6845 (H) x 392.256 (V) (31.51" diagonal)	mm	(1)
Bezel Opening Area	703.8 (H) x 399.0 (V)	mm	
Driver Element	a-si TFT active matrix	-	
Pixel Number	1366 x R.G.B. x 768	pixel	
Pixel Pitch (Sub Pixel)	0.17025(H) x 0.51075 (V)	mm	
Pixel Arrangement	RGB vertical stripe	-	
Display Colors	16.7M	color	
Display Operation Mode	Transmissive mode / Normally black	-	
Surface Treatment	Anti-Glare coating (Haze 11%),Hard coating (3H)	-	

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	759	760	761	mm	(1)
	Vertical(V)	449	450	451	mm	(1)
	Depth(D)	31.5	32.5	33.5	mm	To Rear
	Depth(D)	46.9	47.9	48.9	mm	To Inverter Cover
Weight			5189			g

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions.

2. ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1)
Operating Ambient Temperature	T_{OP}	0	+50	ºC	(1), (2)
Shock (Non-Operating)	S_{NOP}	-	50	G	(3), (5)
Vibration (Non-Operating)	V_{NOP}	-	1.0	G	(4), (5)

Note (1) Temperature and relative humidity range is shown in the figure below.

(a) 90 %RH Max. (Ta ≦ 40 ºC).

(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).

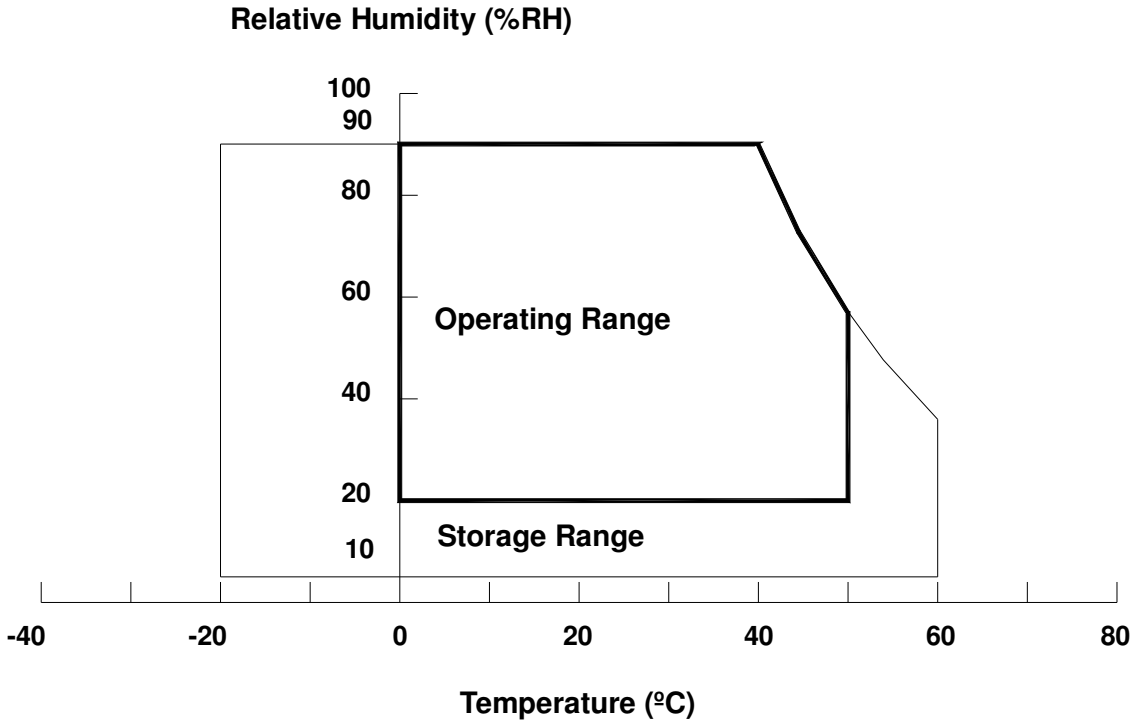
(c) No condensation.

Note (2) The maximum operating temperature is based on the test condition that the surface temperature of display area is less than or equal to 65 ºC with LCD module alone in a temperature controlled chamber. Thermal management should be considered in final product design to prevent the surface temperature of display area from being over 65 ºC. The range of operating temperature may degrade in case of improper thermal management in final product design.

Note (3) 11 ms, half sine wave, 1 time for ± X, ± Y, ± Z.

Note (4) 10 ~ 200 Hz, 10 min, 1 time each X, Y, Z.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.



2.2 Package storage

When storing modules as spares for a long time, the following precaution is necessary.

(a) Do not leave the module in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35℃at normal humidity without condensation.

(b)The module shall be stored in dark place. Do not store the TFT-LCD module in direct sunlight or fluorescent light.

2.3 ELECTRICAL ABSOLUTE RATINGS

2.3.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	Vcc	-0.3	13.5	V	(1)
Input Signal Voltage	V_{IN}	-0.3	3.6	V	

2.3.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Lamp Voltage	V_W	—	3000	V_{RMS}	
Power Supply Voltage	V_{BL}	0	30	V	(1)
Control Signal Level	—	-0.3	7	V	(1), (3)

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Functional operation should be restricted to the conditions described under normal operating conditions.

Note (2) No moisture condensation or freezing.

Note (3)The control signals include On/Off Control, External PWM Control and DET_5V signal for inverter status output.

3. ELECTRICAL CHARACTERISTICS

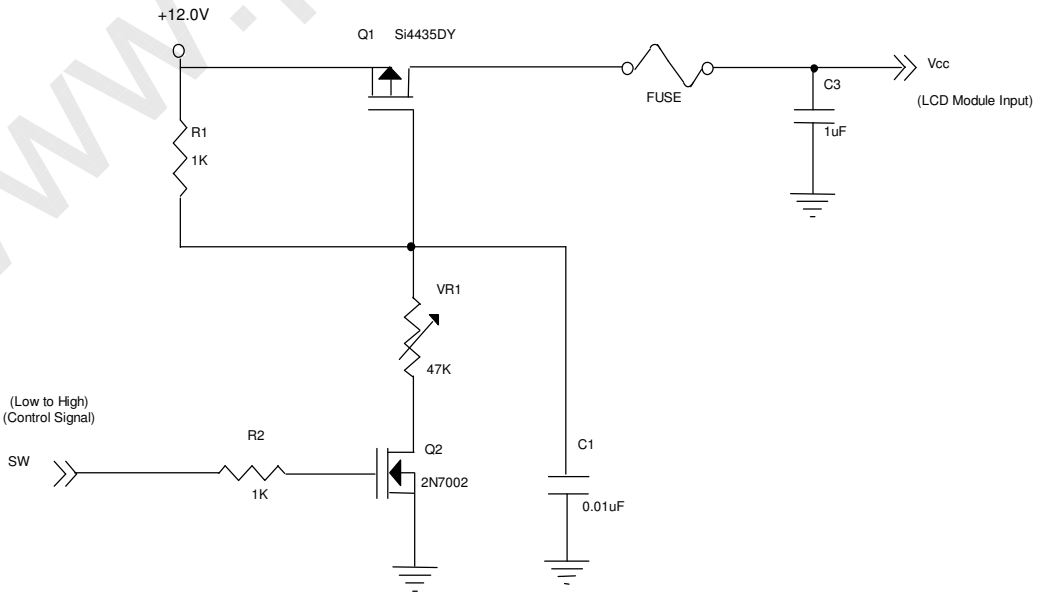
3.1 TFT LCD MODULE

Ta = 25 ± 2 ºC

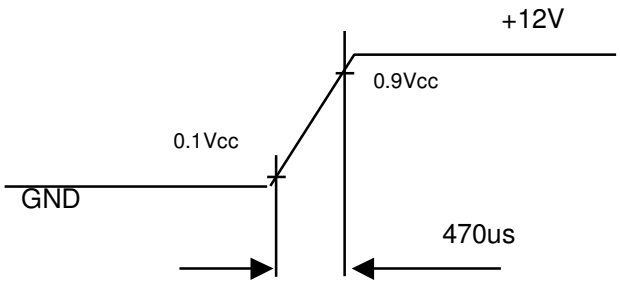
Parameter		Symbol	Value			Unit	Note
			Min.	Typ.	Max.		
Power Supply Voltage		V_{CC}	10.8	12	13.2	V	(1)
Rush Current		I_{RUSH}	–	–	3.3	A	(2)
Power Supply Current	White Pattern	–	–	0.56	–	A	(3)
	Horizontal Stripe	–	–	0.72	0.87	A	
	Black Pattern	–	–	0.40	–	A	
LVDS interface	Differential Input High Threshold Voltage	V_{LVTH}	+100	–	–	mV	(4)
	Differential Input Low Threshold Voltage	V_{LVTL}	–	–	-100	mV	
	Common Input Voltage	V_{CM}	1.0	1.2	1.4	V	
	Differential input voltage (single-end)	$\|V_{ID}\|$	200	–	600	mV	
	Terminating Resistor	R_T	–	100	–	ohm	
CMOS interface	Input High Threshold Voltage	V_{IH}	2.7	–	3.3	V	
	Input Low Threshold Voltage	V_{IL}	0	–	0.7	V	

Note (1) The module should be always operated within above ranges.

Note (2) Measurement Conditions:

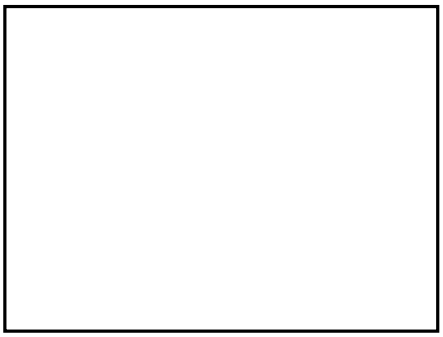


Vcc rising time is 470us



Note (3) The specified power supply current is under the conditions at Vcc =12V, Ta = 25 ± 2 ºC, f_v = 60 Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern

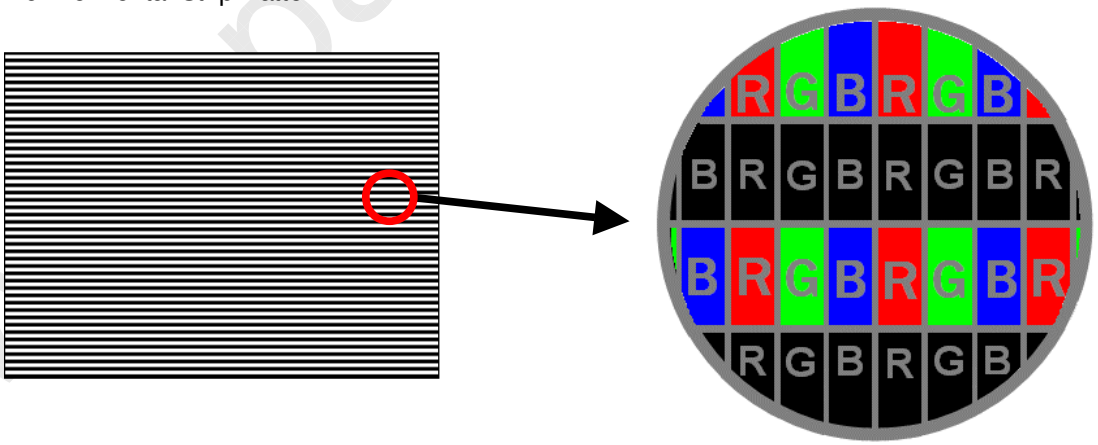


Active Area

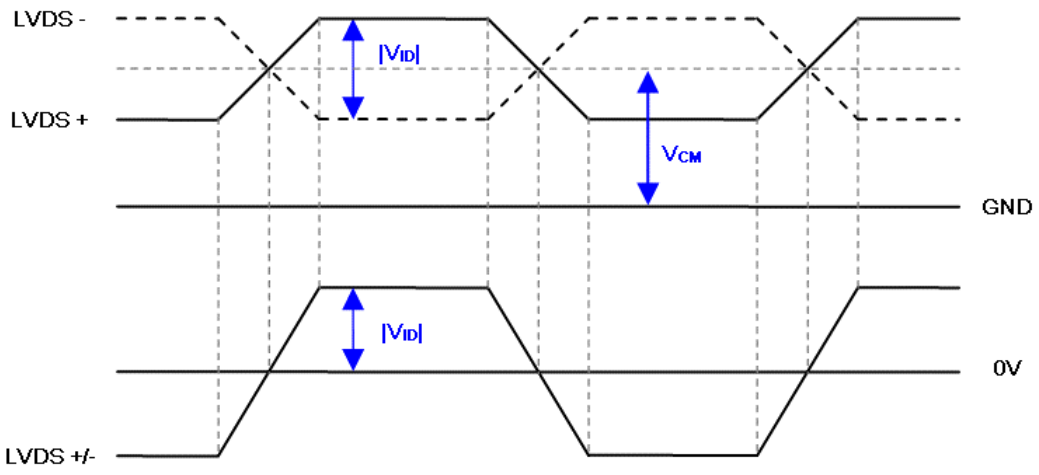
b. Black Pattern

Active Area

c. Horizontal Strip Pattern



Note (4) The LVDS input characteristics are as follows:



3.2 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

3.2.1 CCFL (Cold Cathode Fluorescent Lamp) CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Lamp Input Voltage	V_L	-	1560	-	V_{RMS}	
Lamp Current	I_L	11.8	12.3	12.8	mA_{RMS}	(1)
Lamp Turn On Voltage	V_S	-	-	2710	V_{RMS}	Ta = 0 ºC (2)
		-	-	2260	V_{RMS}	Ta = 25 ºC (2)
Operating Frequency	F_L	40	-	70	KHz	
Lamp Life Time	L_{BL}	50,000	60,000	-	Hrs	(4)

3.2.2 INVERTER CHARACTERISTICS (Ta = 25 ± 2 ºC)

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Total Power Consumption	P_{BL}	-	74	78	W	(5), (6), I_L =12.3mA
Power Supply Voltage	V_{BL}	22.8	24	25.2	V_{DC}	
Power Supply Current	I_{BL}	-	3.08	3.25	A	Non Dimming
Input Ripple Noise	-	-	-	912	mV_{P-P}	V_{BL}=22.8V
Oscillating Frequency	F_W	60	63	66	kHz	(3)
Dimming frequency	F_B	150	160	170	Hz	
Minimum Duty Ratio	D_{MIN}	10	20	-	%	(7)

Note (1) Lamp current is measured by utilizing AC current probe and its value is average by measuring master and slave board.

Note (2) The lamp starting voltage V_S should be applied to the lamp for more than 1 second after startup. Otherwise the lamp may not be turned on.

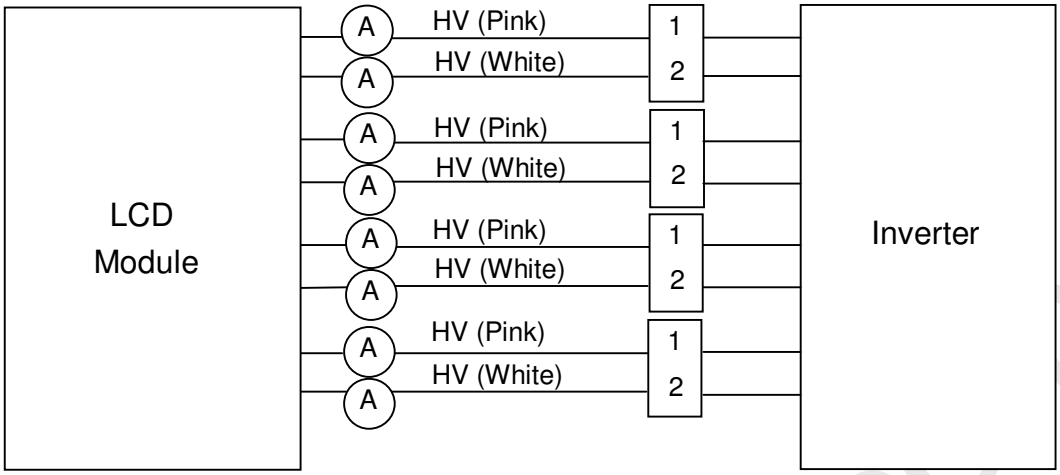
Note (3) The lamp frequency may produce interference with horizontal synchronous frequency of the display input signals, and it may result in line flow on the display. In order to avoid interference, the lamp frequency should be detached from the horizontal synchronous frequency and its harmonics as far as possible.

Note (4) The life time of a lamp is defined as when the brightness is larger than 50% of its original value and the effective discharge length is longer than 80% of its original length (Effective discharge length is defined as an area that has equal to or more than 70% brightness compared to the brightness at the center point of lamp.) as the time in which it continues to operate under the condition at Ta = 25 ±2℃ and I_L = 11.8~ 12.8mArms.

Note (5) The power supply capacity should be higher than the total inverter power consumption P_{BL}. Since the pulse width modulation (PWM) mode was applied for backlight dimming, the driving current changed as PWM duty on and off. The transient response of power supply should be considered for the changing loading when inverter dimming.

Note (6) The measurement condition of Max. value is based on 31.5" backlight unit under input voltage 24V, average lamp current 12.6 mA and lighting 30 minutes later.

Note (7) 10% minimum duty ratio is only valid for electrical operation



3.2.3 INVERTER INTERFACE CHARACTERISTICS

ITEM		SYMBOL	TEST CONDITION	MIN	TYPE	MAX	UNIT	NOTE
DET_5V		DET_5V	–	4.5	5.0	5.5	V	Abnormal
			–	0	–	0.8	V	Normal
On/Off Control Voltage	ON	V_{BLON}	–	3.3	–	5.3	V	
	OFF		–	0	–	0.8	V	
External PWM Control Voltage	HI	V_{EPWM}	–	3.5	–	5.3	V	Duty on
	LO		–	0	–	0.8	V	Duty off
Control Signal Rising Time		Tr	–	–	–	100	ms	
Control Signal Falling Time		Tf	–	–	–	100	ms	
VBL Rising Time		Tr1	–	30	–	–	ms	10%-90%V_{BL}
VBL Falling Time		Tf1	–	30	–	–	ms	
PWM Signal Rising Time		T_{PWMR}	–	–	–	100	us	
PWM Signal Falling Time		T_{PWMF}	–	–	–	100	us	
Input impedance		R_{IN}	–	1	–	–	MΩ	
PWM Delay Time		T_{PWM}	–	100		–	mS	
BLON Delay Time		T_{on}	–	300	–	–	mS	
		T_{on1}		300	–	–	mS	
BLON Off Time		T_{OFF}	–	300	–	–	mS	

Note (1) The Dimming signal should be valid before backlight turns on by BLON signal. It is inhibited to change the internal/external PWM signal during backlight turn on period.

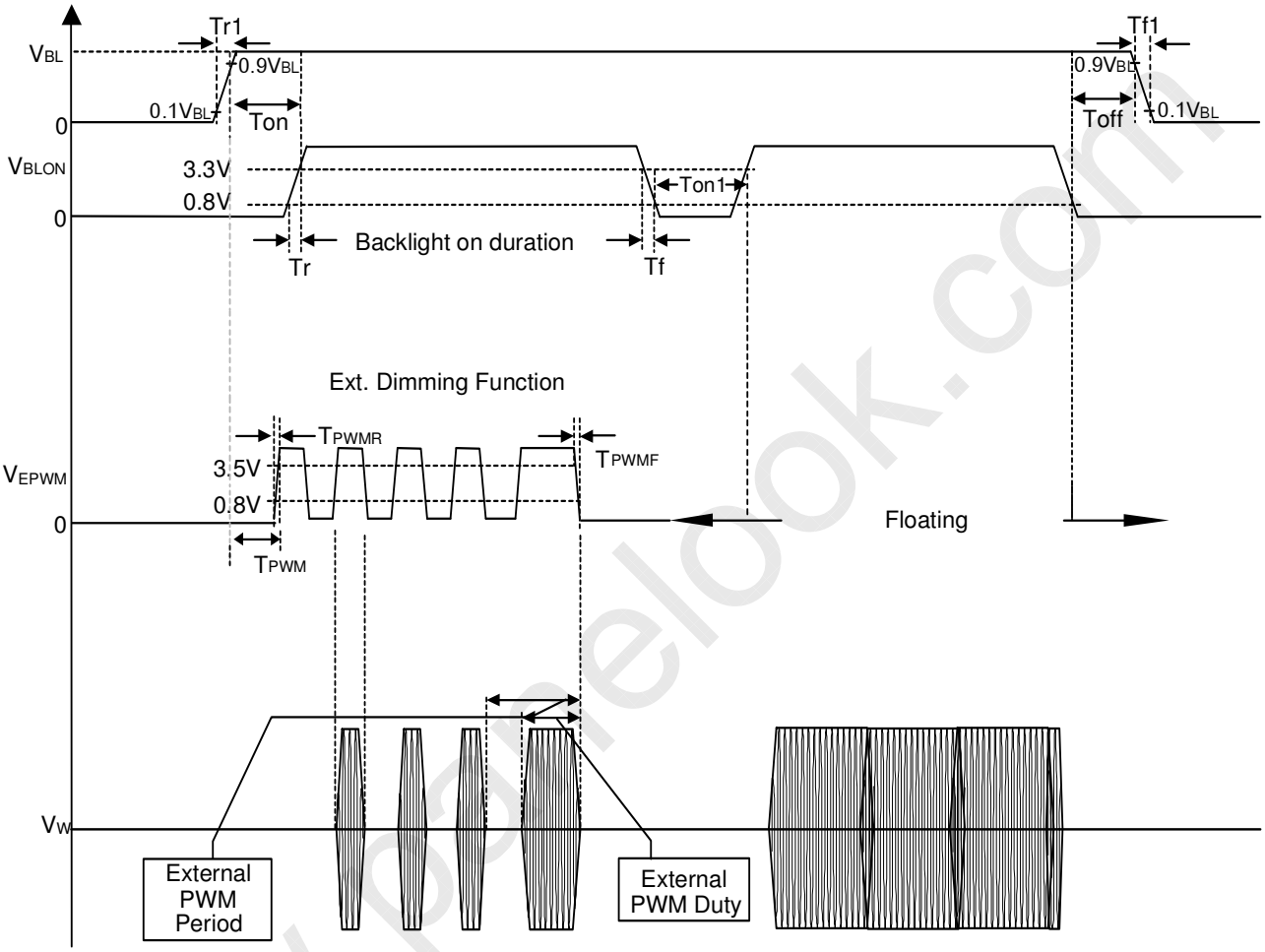
Note (2) The power sequence and control signal timing are shown in the following figure. For a certain reason, the inverter has a possibility to be damaged with wrong power sequence and control

signal timing.

Note (3) While system is turned ON or OFF, the power sequences must follow as below descriptions:

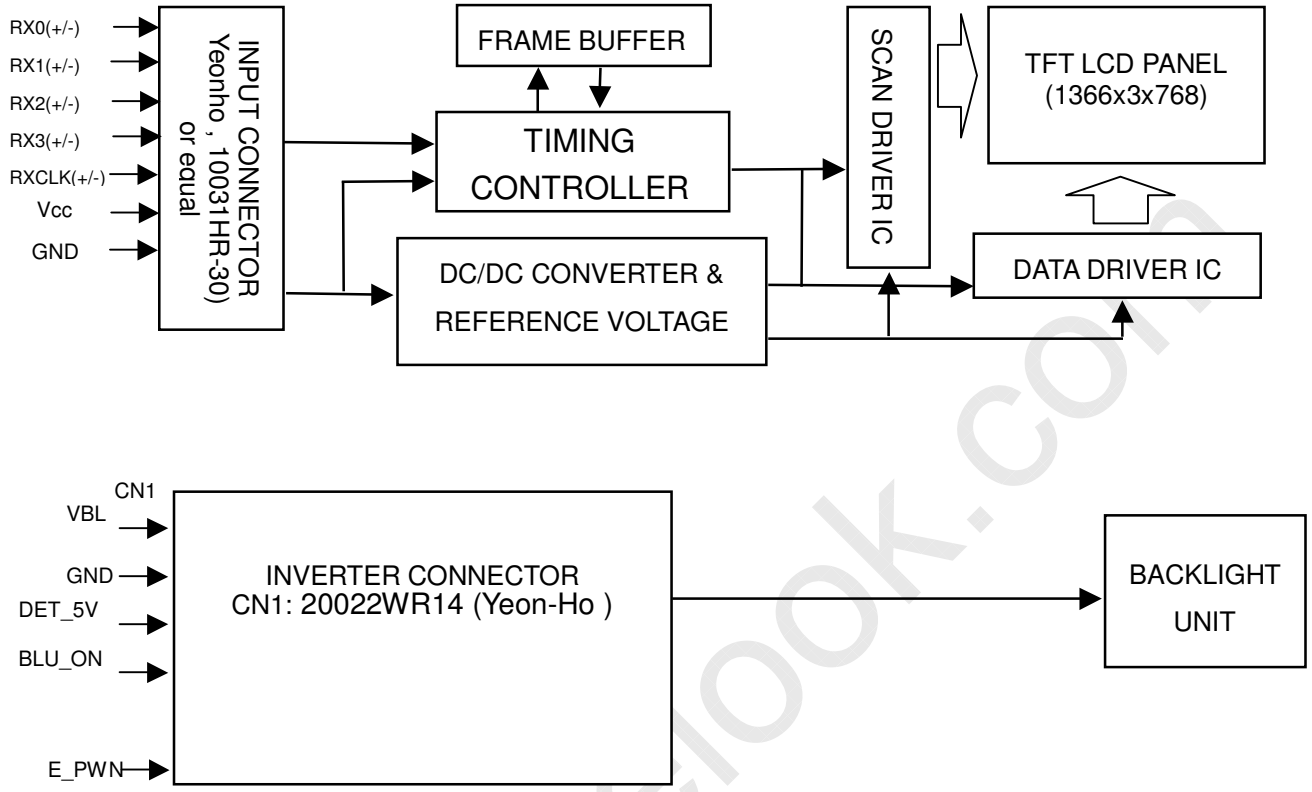
Turn ON sequence: VBL → PWM signal → BLON

Turn OFF sequence: BLOFF → PWM signal → VBL



4. BLOCK DIAGRAM

4.1 TFT LCD MODULE



5. INTERFACE PIN CONNECTION

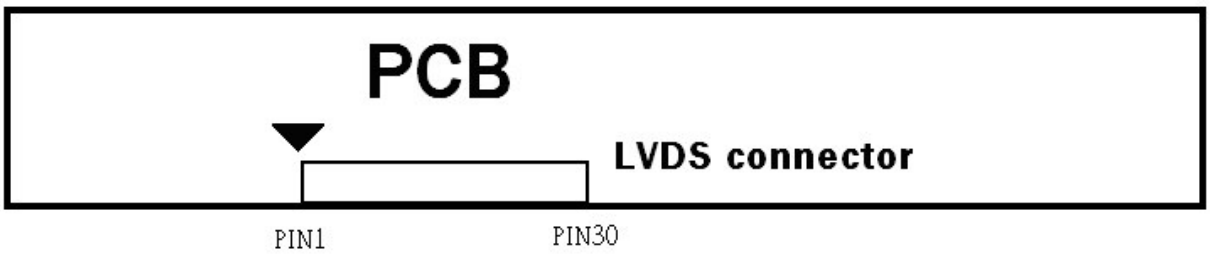
5.1 TFT LCD MODULE

CNF1 Connector Pin Assignment

Pin No.	Symbol	Description	Note
1	NC	No connection	(3)
2	SCL	EEPROM Serial Clock	
3	SDA	EEPROM Serial Data	
4	GND	Ground	
5	RX0-	Negative transmission data of pixel 0	
6	RX0+	Positive transmission data of pixel 0	
7	GND	Ground	
8	RX1-	Negative transmission data of pixel 1	
9	RX1+	Positive transmission data of pixel 1	
10	GND	Ground	
11	RX2-	Negative transmission data of pixel 2	
12	RX2+	Positive transmission data of pixel 2	
13	GND	Ground	
14	RXCLK-	Negative of clock	
15	RXCLK+	Positive of clock	
16	GND	Ground	
17	RX3-	Negative transmission data of pixel 3	
18	RX3+	Positive transmission data of pixel 3	
19	GND	Ground	
20	NC	No connection	(3)
21	SELLVDS	Select LVDS data format	(2)(4)
22	WP	EEPROM Write Protection	
23	GND	Ground	
24	GND	Ground	
25	GND	Ground	
26	VCC	Power supply: +12V	
27	VCC	Power supply: +12V	
28	VCC	Power supply: +12V	
29	VCC	Power supply: +12V	
30	VCC	Power supply: +12V	

Note (1) Connector type: 10031HR-30 (Yeonho) or compatible

LVDS connector pin orderdefined as follows



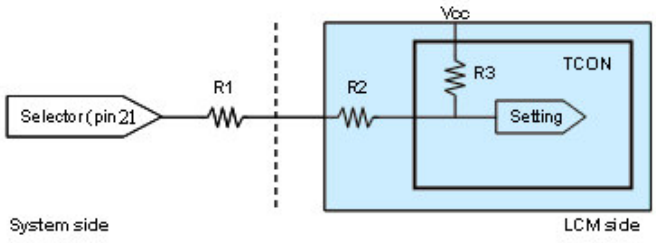
Note (2) HIGH = Connect to +3.3V or OPEN : VESA, LOW = connect to GND : JEIDA LVDS format

Please refer to 5.4 LVDS INTERFACE

Note (3) Reserved for internal use. Left it open.

Note (4) LVDS signal pin connected to the LCM side has the following diagram.

R1 in the system side should be less than 1K Ohm. (R1 < 1K Ohm)



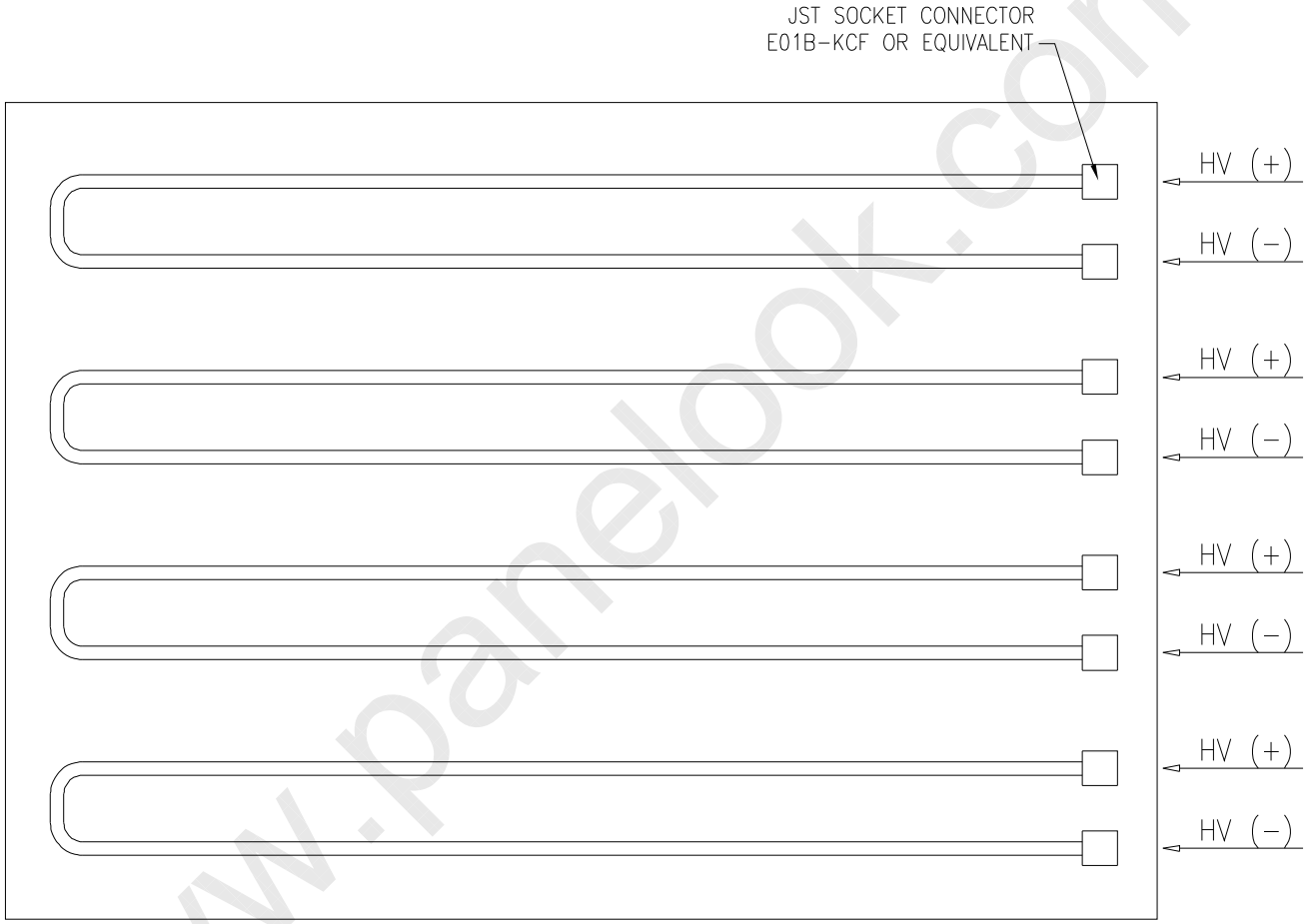
5.2 BACKLIGHT UNIT

The pin configuration for the housing and leader wire is shown in the table below.

CN2-CN5 (Socket Connector): E01B-KCF or equivalent

Pin No.	Symbol	Description	Remark
1	HV	High Voltage	
	HV	High Voltage	

Note (1) The backlight interface housing for high voltage side is a model E01B-KCF, manufactured by JST or equivalent.

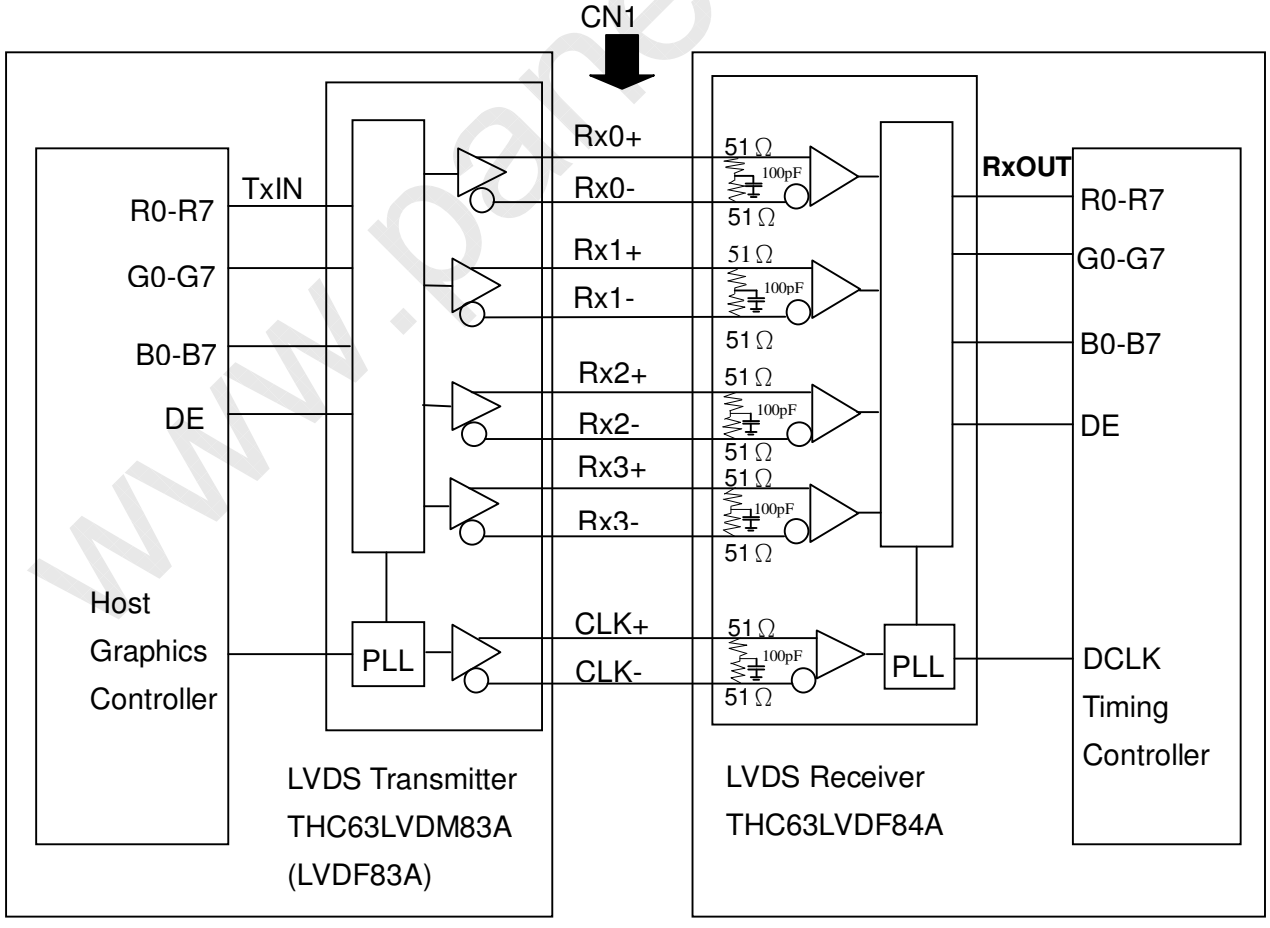


5.3 INVERTER UNIT

CN1(Header): 20022WR14 (Yeon-Ho)

Pin No.	Symbol	Description
1	VBL	+24V Power input
2		
3		
4		
5		
6	GND	Ground
7		
8		
9		
10		
11	DET_5V	Check Lamp Ignition.
12	BLU_ON	BL ON/OFF
13	N.C.	No connect.
14	E_PWM	External PWM Control

5.3 BLOCK DIAGRAM OF INTERFACE

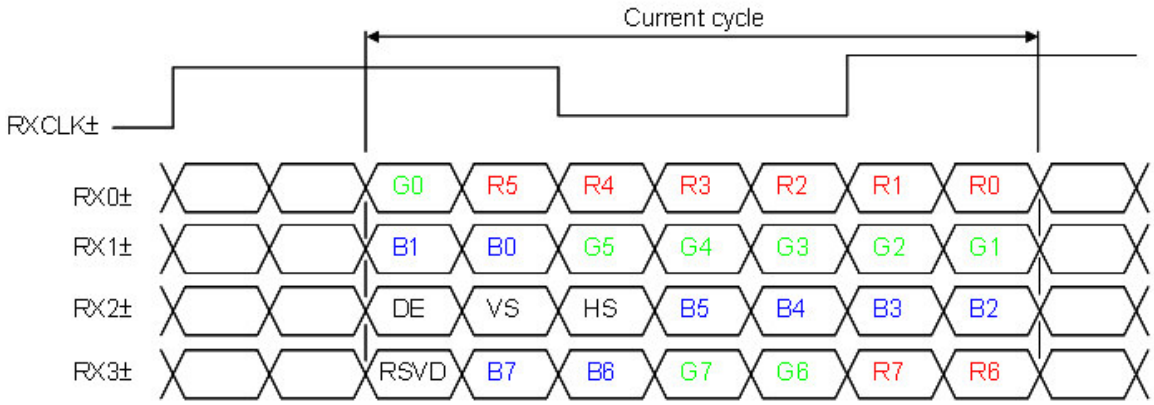


R0~R7 : Pixel R Data ,
G0~G7 : Pixel G Data ,
B0~B7 : Pixel B Data ,
DE : Data enable signal

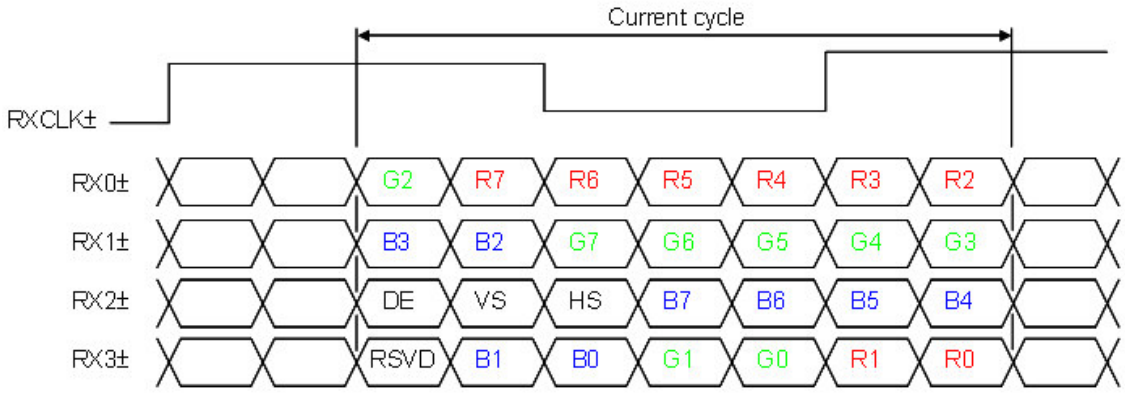
Note (1) The system must have the transmitter to drive the module.
Note (2) LVDS cable impedance shall be 50 ohms per signal line or about 100 ohms per twist-pair line when it is used differentially.

5.4 LVDS INTERFACE

VESA LVDS format：(SELLVDS pin=H or open)



JEDIA LVDS format：(SELLVDS pin=L)



R0~R7: Pixel R Data (7; MSB, 0; LSB)
G0~G7: Pixel G Data (7; MSB, 0; LSB)
B0~B7: Pixel B Data (7; MSB, 0; LSB)
DE: Data enable signal
Notes(1) RSVD(reserved)pins on the transmitter shall be “H” or(“L” or OPEN)

5.5 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																							
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

6. INTERFACE TIMING

6.1 INPUT SIGNAL TIMING SPECIFICATIONS

The input signal timing specifications are shown as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
LVDS Receiver Clock	Frequency	F_{clkin} (=1/TC)	60	76	82	MHz	
	Input cycle to cycle jitter	T_{rcl}	—	—	200	ps	(3)
	Spread spectrum modulation range	F_{clkin_mod}	F_{clkin}-2%	—	F_{clkin}+2%	MHz	(4)
	Spread spectrum modulation frequency	F_{SSM}			200	KHz	
LVDS Receiver Data	Setup Time	Tlvsu	600	—	—	ps	(5)
	Hold Time	Tlvhd	600	—	—	ps	
Vertical Active Display Term	Frame Rate	F_{r5}	47	50	53	Hz	
		F_{r6}	57	60	63	Hz	
	Total	Tv	778	806	888	Th	Tv=Tvd+Tvb
	Display	Tvd	768	768	768	Th	—
	Blank	Tvb	10	38	120	Th	—
Horizontal Active Display Term	Total	Th	1442	1560	1936	Tc	Th=Thd+Thb
	Display	Thd	1366	1366	1366	Tc	—
	Blank	Thb	76	194	570	Tc	—

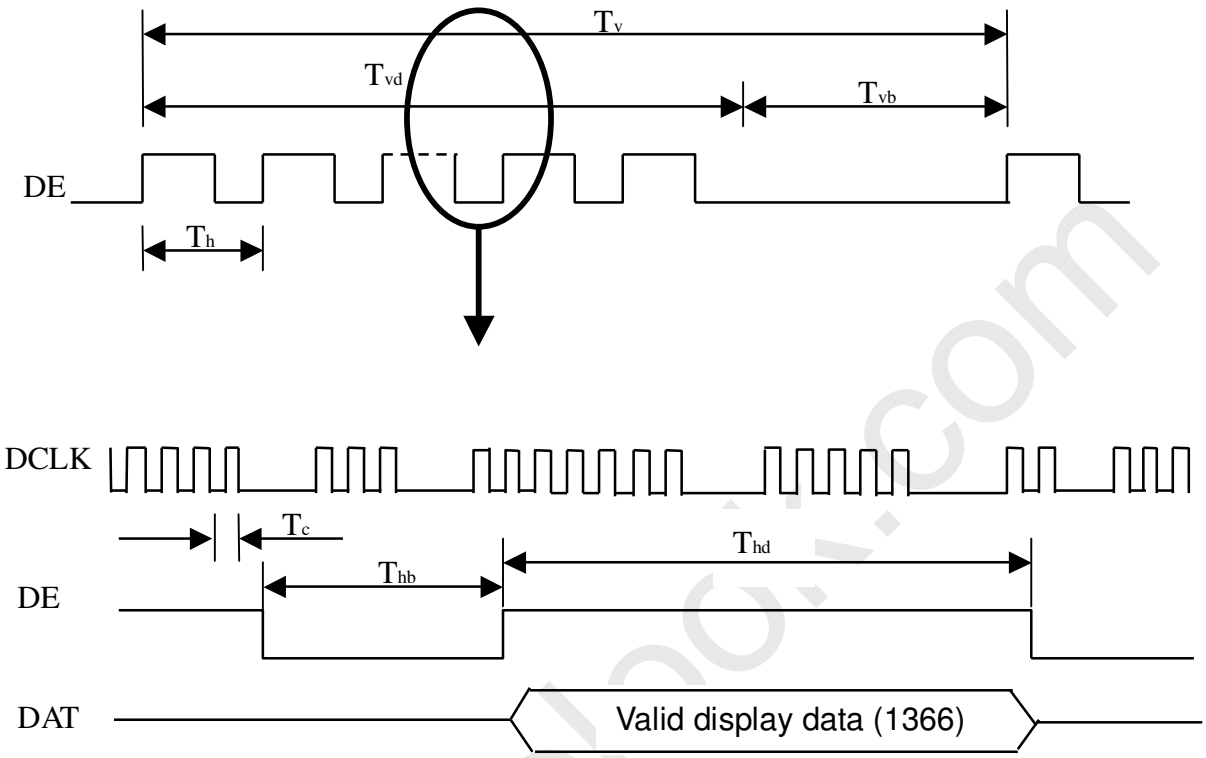
Note (1) Please make sure the range of pixel clock has follow the below equation :

$F_{clkin(max)} \geqq F_{r6} \times Tv \times Th$

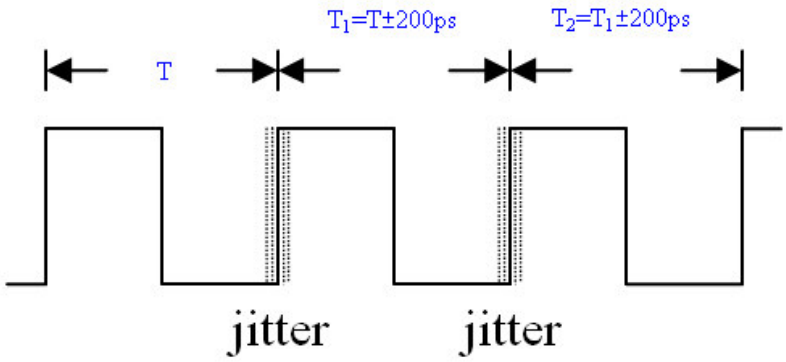
$F_{r5} \times Tv \times Th \geqq F_{clkin(min)}$

Note (2) This module is operated in DE only mode and please follow the input signal timing diagram below :

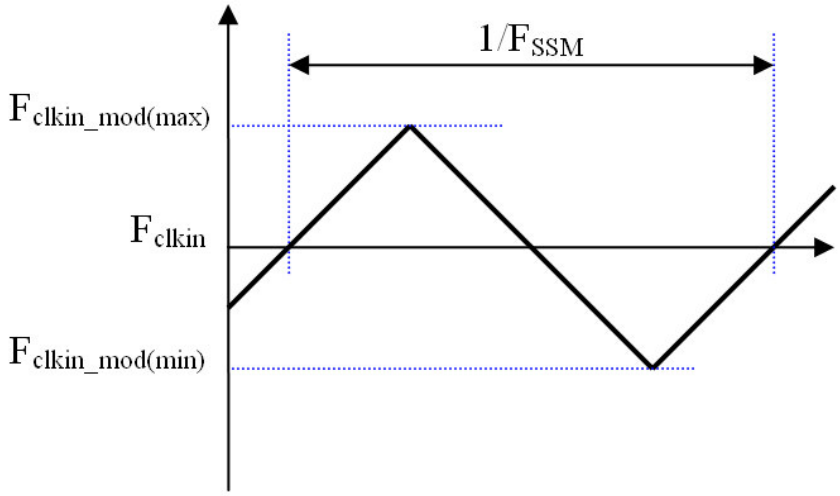
INPUT SIGNAL TIMING DIAGRAM



Note (3) The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI

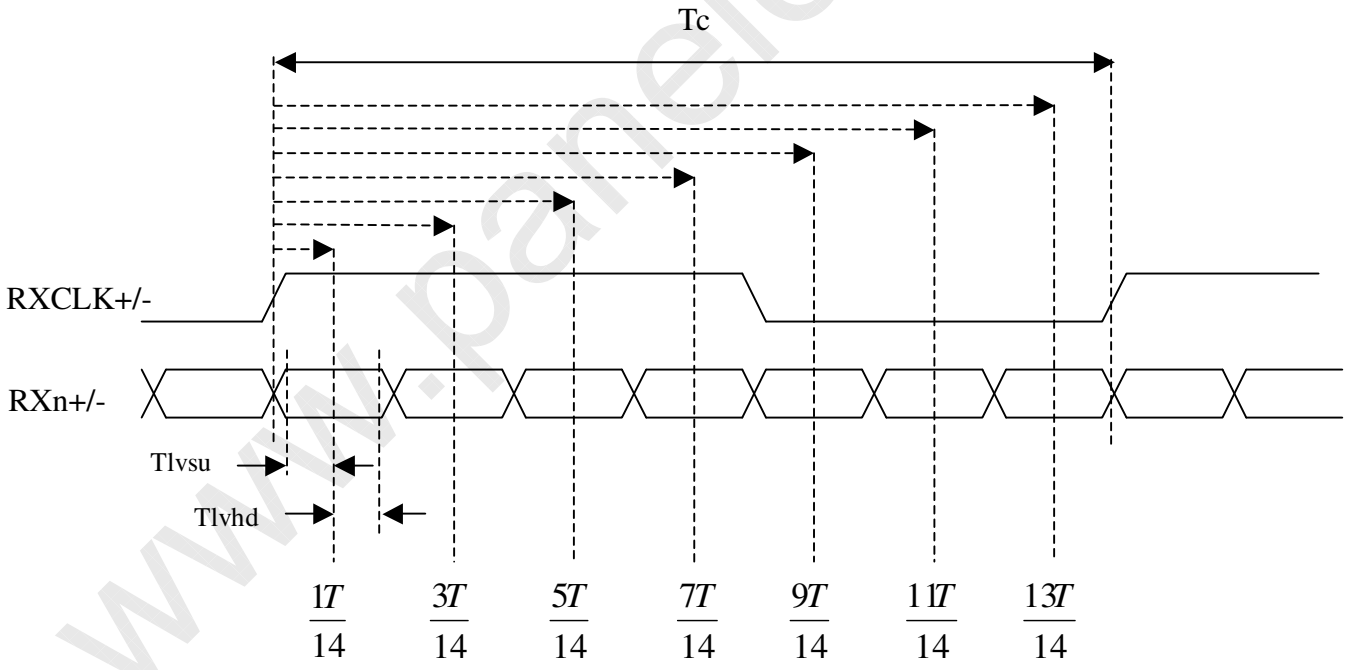


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



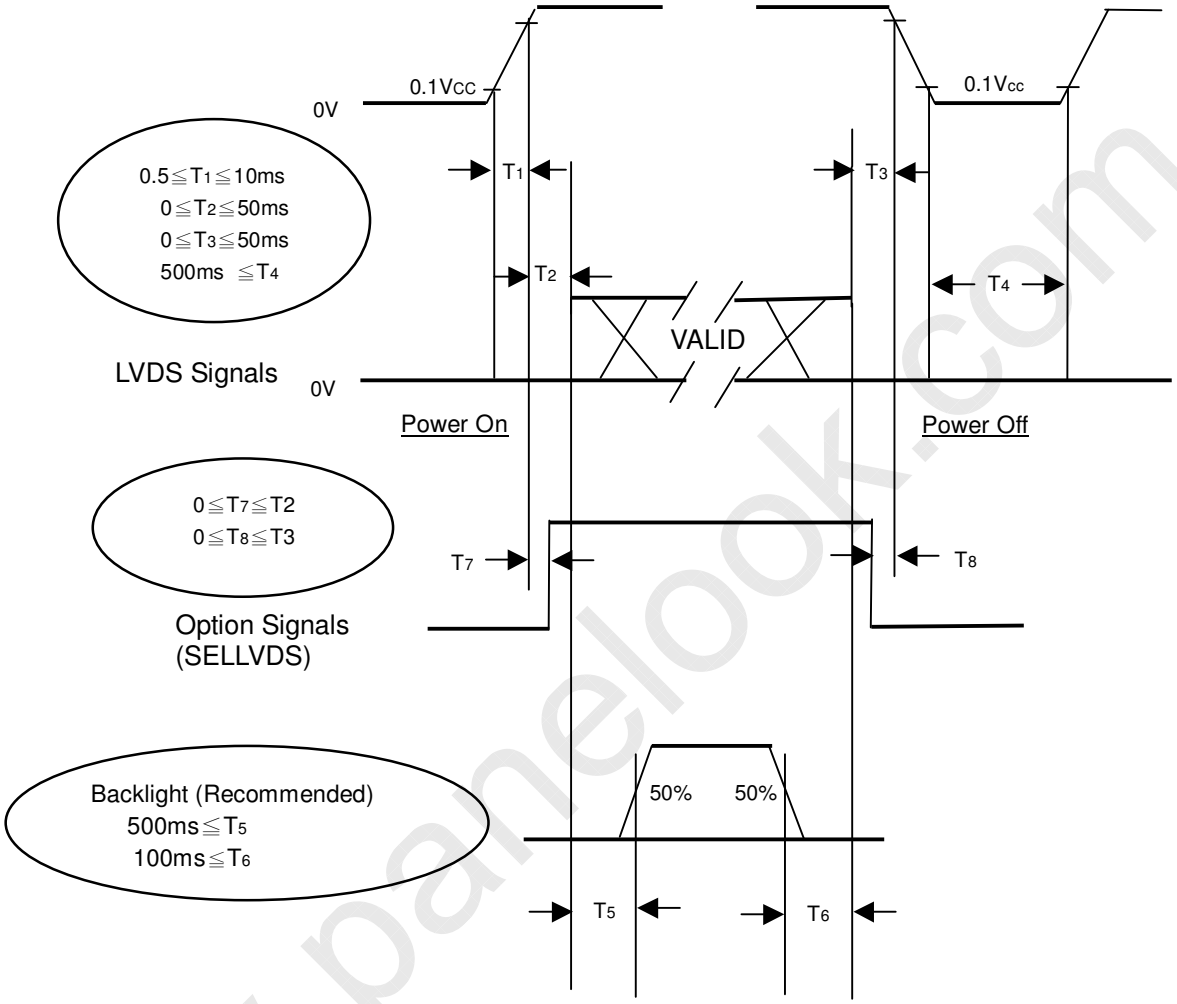
Note (5) The LVDS timing diagram and setup/hold time is defined and showing as the following figures.

LVDS RECEIVER INTERFACE TIMING DIAGRAM



6.2 POWER ON/OFF SEQUENCE

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Power ON/OFF Sequence

Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the lamp voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen.

Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0, that maybe cause electrical overstress failures.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period.

Note (5) Interface signal shall not be kept at high impedance when the power is on.

7. OPTICAL CHARACTERISTICS

7.1 TEST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{CC}	12.0	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
Lamp Current	I_L	12.3±0.5	mA
Oscillating Frequency (Inverter)	F_W	63±3	KHz
Frame rate	Fr	60	Hz

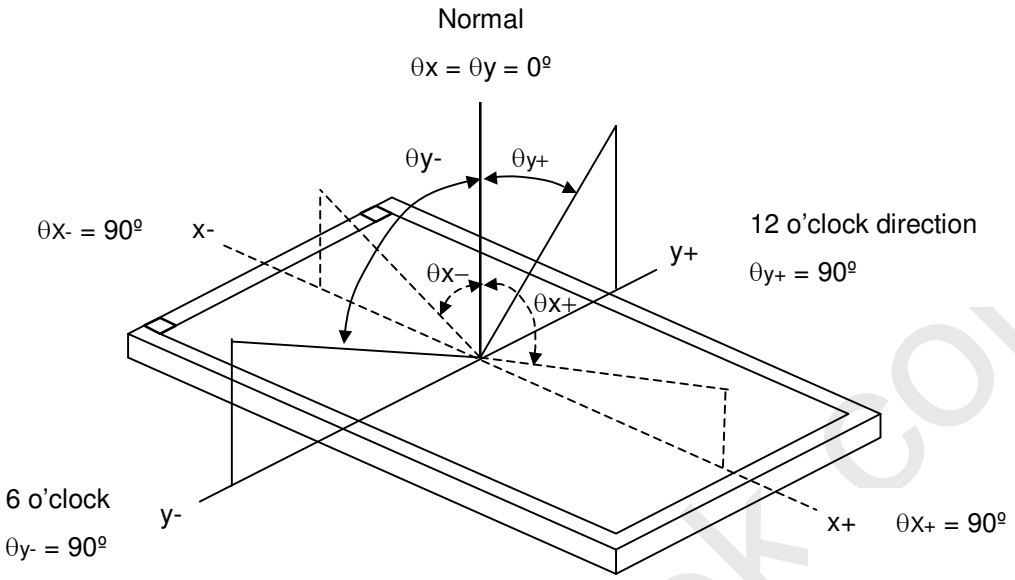
7.2 OPTICAL SPECIFICATIONS

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	θ_x=0°, θ_Y =0° Viewing Angle at Normal Direction	2600	3500	-	-	(2)
Response Time		Gray to gray average			8.5	14	ms	(3)
Center Luminance of White		L_C		360	450	-	cd/m^2	(4)
White Variation		δW		-	-	1.3	-	(7)
Cross Talk		CT		-	-	4.0	%	(5)
Color Chromaticity	Red	Rx		Typ -0.03	0.648	Typ +0.03	-	(6)
		Ry			0.331		-	
	Green	Gx			0.272		-	
		Gy			0.601		-	
	Blue	Bx			0.143		-	
		By			0.064		-	
	White	Wx			0.280		-	
		Wy			0.290		-	
	Color Gamut	CG			72		%	NTSC
Viewing Angle	Horizontal	θ_x+	CR≥20	80	88	-	Deg.	(1)
		θ_x-		80	88	-		
	Vertical	θ_Y+		80	88	-		
		θ_Y-		80	88	-		

Note (1) Definition of Viewing Angle (θx, θy):

Viewing angles are measured by Autronic Conoscope Cono-80.



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

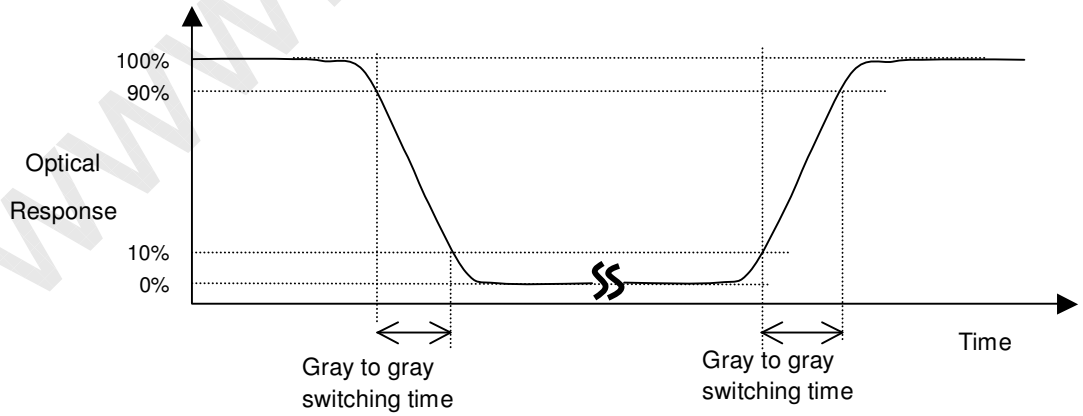
Contrast Ratio (CR) = L255 / L0

L255: Luminance of gray level 255

L 0: Luminance of gray level 0

CR = CR (5), where CR (X) is corresponding to the Contrast Ratio of the point X at the figure in Note (7).

Note (3) Definition of Gray to Gray Switching Time :



The driving signal means the signal of luminance 0%, 20%, 40%, 60%, 80%, 100%.

Gray to gray average time means the average switching time of luminance 0%,20%,

40%, 60%, 80%, 100% to each other.

Note (4) Definition of Luminance of White (L_C, L_{AVE}):

Measure the luminance of gray level 255 at center point and 5 points

$L_C = L(5)$

$L_{AVE} = [L(1)+ L(2)+ L(3)+ L(4)+ L(5)] / 5$

where L (x) is corresponding to the luminance of the point X at the figure in Note (7).

Note (5) Definition of Cross Talk (CT):

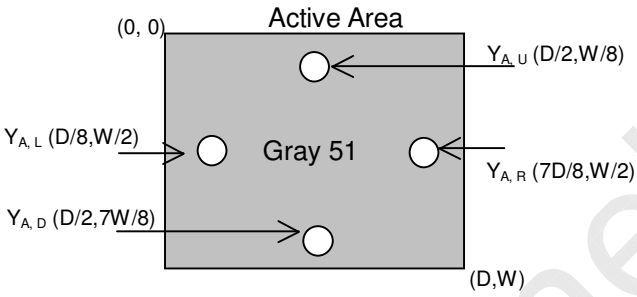
$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

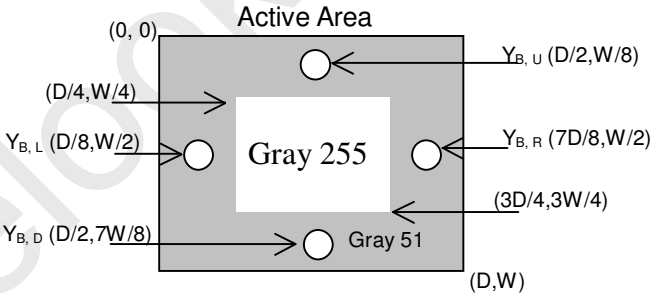
Where:

(a)

Y_A = Luminance of measured location without gray level 255 pattern (cd/m^2)

Y_B = Luminance of measured location with gray level 255 pattern (cd/m^2)

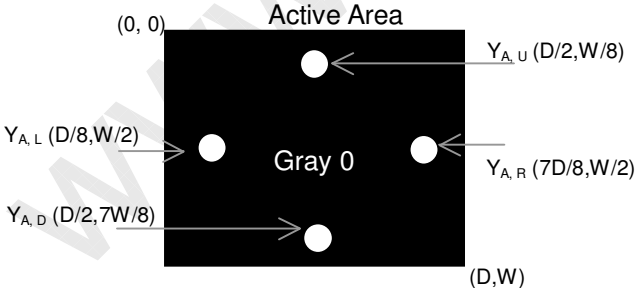


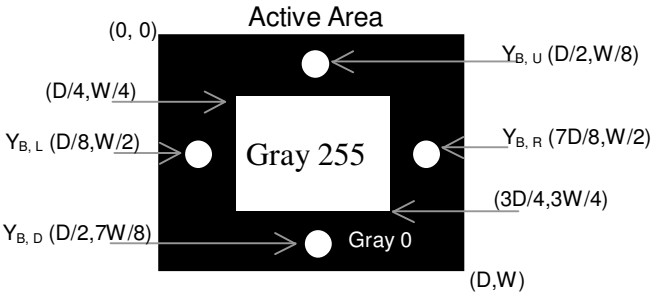


(b)

Y_A = Luminance of measured location without gray level 255 pattern (cd/m^2)

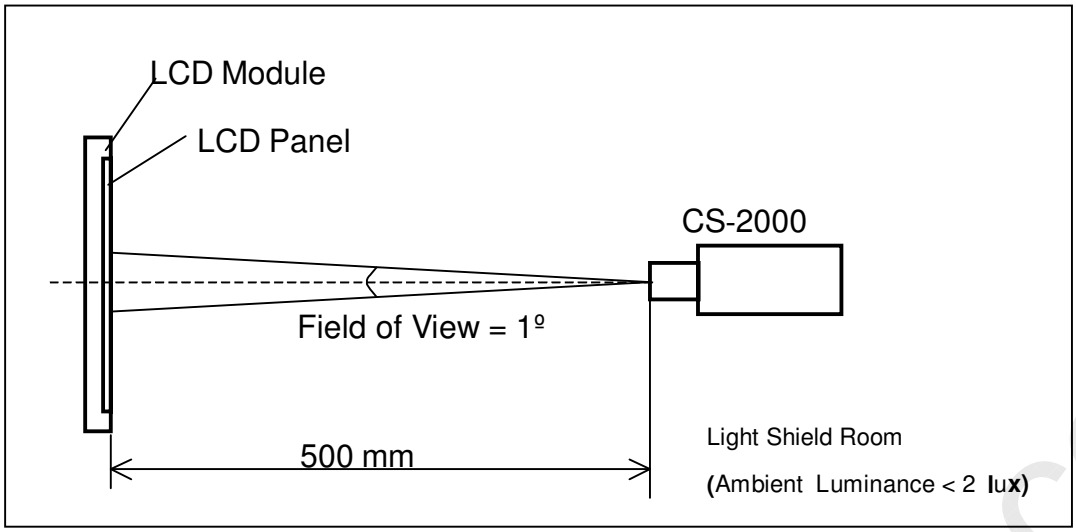
Y_B = Luminance of measured location with gray level 255 pattern (cd/m^2)





Note (6) Measurement Setup:

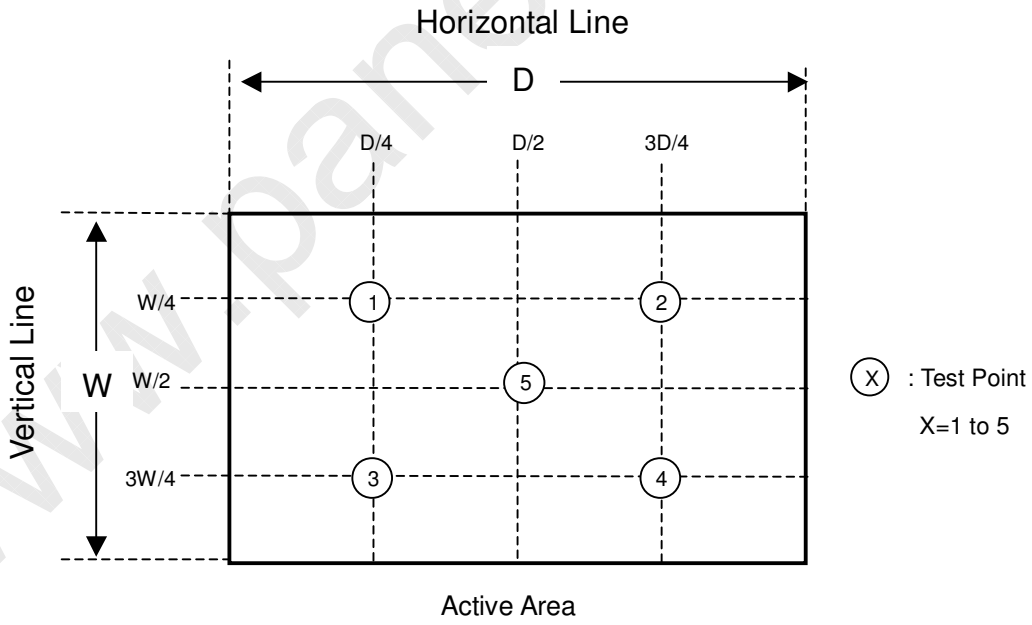
The LCD module should be stabilized at given temperature for 1 hour to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 1 hour in a windless room.



Note (7) Definition of White Variation (δW):

Measure the luminance of gray level 255 at 5 points

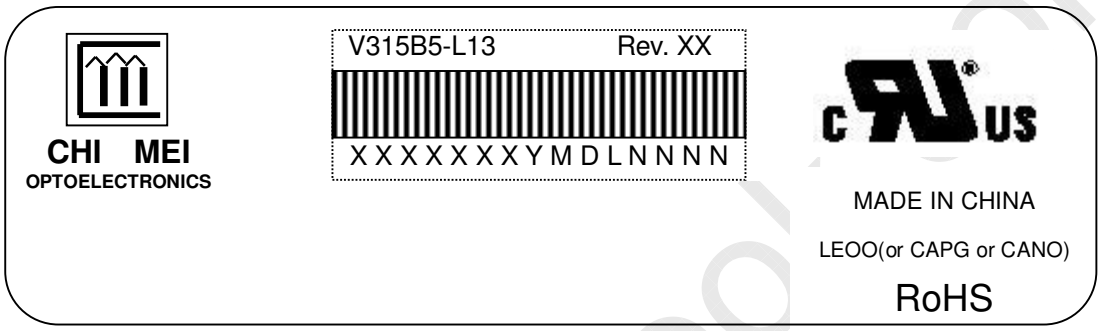
δW = Maximum [L (1), L (2), L (3), L (4), L (5)] / Minimum [L (1), L (2), L (3), L (4), L (5)]



8. DEFINITION OF LABELS

8.1 CMO MODULE LABEL

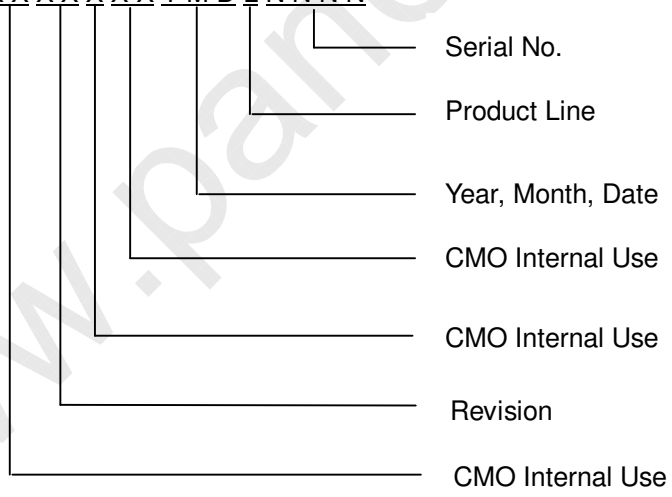
The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



(a) Model Name: V315B5-L13

(b) Revision: Rev. XX, for example: A0, A1… B1, B2… or C1, C2…etc.

(c) Serial ID: X X X X X X X Y M D L N N N N



9. PACKAGING

9.1 PACKING SPECIFICATIONS

(1) 5 LCD TV modules / 1 Box

(2) Box dimensions : 826(L) X 376 (W) X 540 (H)

(3) Weight : approximately 30Kg (5 modules per box)

9.2 PACKING METHOD

Figures 9-1 and 9-2 are the packing method

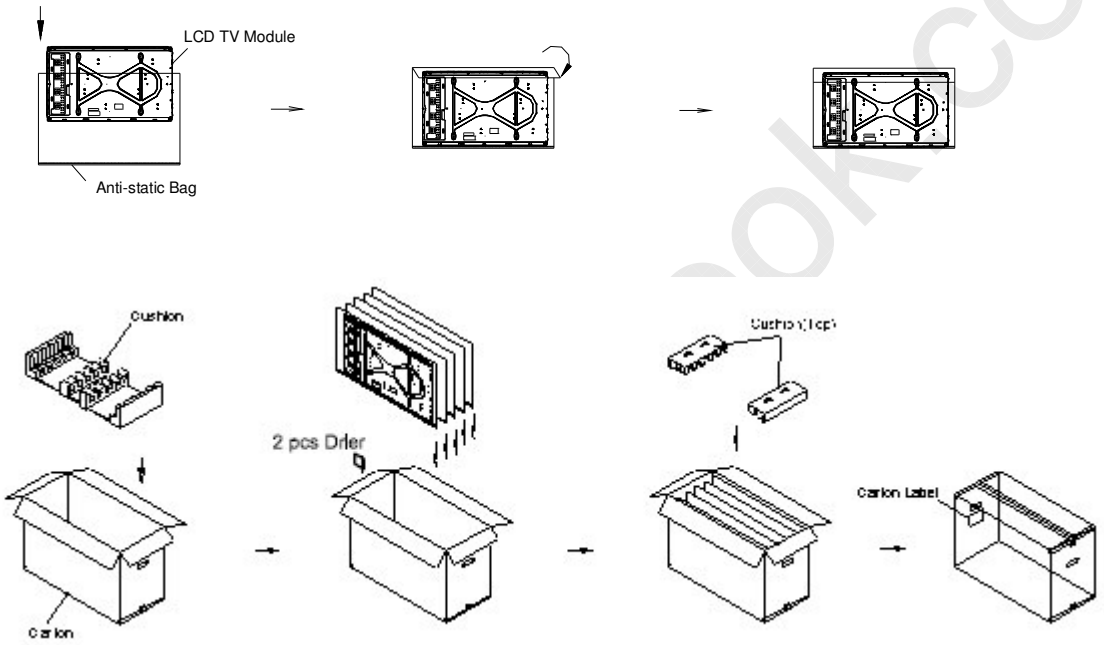


Figure.9-1 packing method

Sea / Land Transportation
(40ft Container)
Gross:285kg

Air Transportation
Gross:195kg

Sea / Land Transportation
(40ft HQ Container)
Gross:390kg

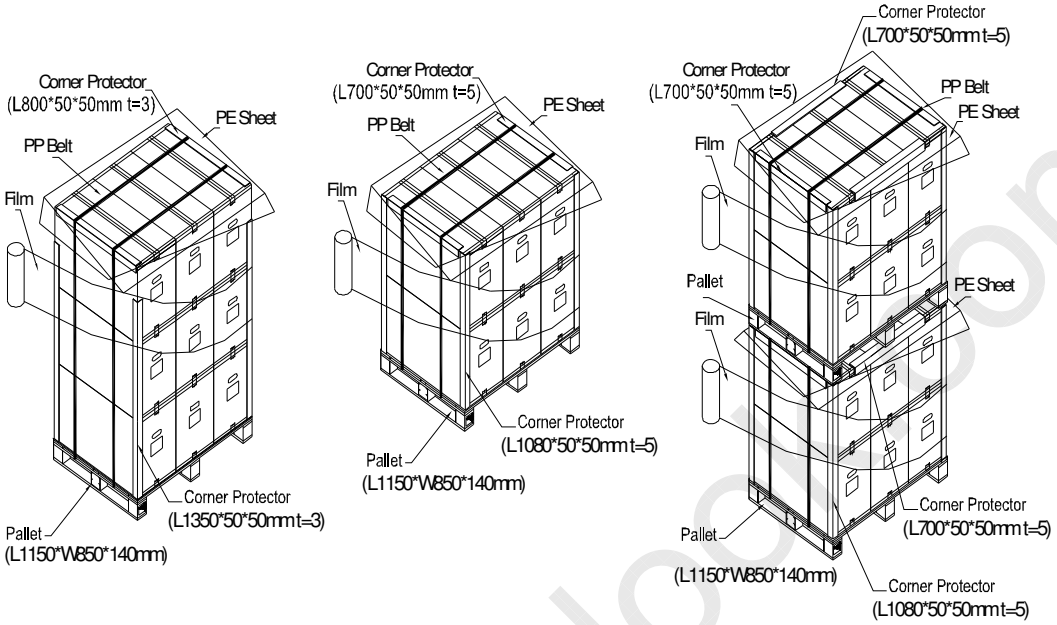


Figure.9-2 packing method

10. PRECAUTIONS

10.1 ASSEMBLY AND HANDLING PRECAUTIONS

(1) Do not apply rough force such as bending or twisting to the module during assembly.

(2) It is recommended to assemble or to install a module into the user's system in clean working areas. The dust and oil may cause electrical short or worsen the polarizer.

(3) Do not apply pressure or impulse to the module to prevent the damage of LCD panel and backlight.

(4) Always follow the correct power-on sequence when the LCD module is turned on. This can prevent the damage and latch-up of the CMOS LSI chips.

(5) Do not plug in or pull out the I/F connector while the module is in operation.

(6) Do not disassemble the module.

(7) Use a soft dry cloth without chemicals for cleaning, because the surface of polarizer is very soft and easily scratched.

(8) Moisture can easily penetrate into LCD module and may cause the damage during operation.

(9) High temperature or humidity may deteriorate the performance of LCD module. Please store LCD modules in the specified storage conditions.

(10) When ambient temperature is lower than 10ºC, the display quality might be reduced. For example, the response time will become slow, and the starting voltage of CCFL will be higher than that of room temperature.

10.2 SAFETY PRECAUTIONS

(1) The startup voltage of a backlight is over 1000 Volts. It may cause an electrical shock while assembling with the inverter. Do not disassemble the module or insert anything into the backlight unit.

(2) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, skin or clothes, it has to be washed away thoroughly with soap.

(3) After the module's end of life, it is not harmful in case of normal operation and storage.

11. MECHANICAL CHARACTERISTICS